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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,489	03/23/2004	Kim Yi-tae	SAM-0367DIV	2787

7590 02/09/2005

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EXAMINER

VU, DAVID

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H/A

Office Action Summary

Application No.

10/806,489

Applicant(s)

YI-TAE, KIM

Examiner

DAVID VU

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/345,852.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>04/09/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-10 are rejected under 35 U. S. C. 103(a) as being unpatentable over Applicant admitted Prior Art (AAPA) (See US 2004/0180458) in view of Maegawa et al. (US Pat. 5,191,399, herein after Maegawa).

Regarding claim 1-3, 5, 6 and 8-10, AAPA discloses a method for manufacturing an image sensor having a photo diode, comprising: forming a transfer gate Tg and a reset gate Rg on predetermined portions of a semiconductor substrate 10 with a specific distance therebetween; forming a photoresist pattern exposing a region at one side of the transfer gate; forming spacers 22 on both walls of the transfer gate and the reset gate; and forming a junction region 24/26 by implanting the n-type impurities into a space between the transfer gate and reset gate, and to one side of the reset gate; forming a p-type photo diode region 15 by implanting p-type impurities into the exposed semiconductor substrate with a first ion implantation energy; forming a first n-type photo diode region 20 by implanting first n-type impurities into a portion below the p-type photo diode region, with a second ion implantation energy (fig. 2 and [0010]).

AAPA fails to disclose forming a second n-type photo diode region by implanting second n-type impurities into a portion surrounding the first n-type photo diode region, with a third ion implantation energy.

Maegawa disclose a method for manufacturing an image sensor having a photo diode, comprising: forming a transfer gate 8; forming a photoresist pattern 12 exposing a region at one side of the transfer gate 8 (fig. 6(a)-6(b) and col. 6, lines 10-19); forming a p-type photo diode region 6 by implanting p-type impurities into the exposed semiconductor substrate 1 with a first ion implantation energy; forming a first n-type photo diode region 5' by implanting first n-type impurities into a portion below the p-type photo diode region, with a second ion implantation energy; forming a second n-type photo diode region 9 by implanting second n-type impurities into a portion surrounding the first n-type photo diode region, with a third ion implantation energy (col. 6, lines 20-45 and col. 7, lines 53-55); wherein the second n-type ion implantation energy is greater than the first n-type ion implantation energies (col. 5, lines 6-9 and col. 8, lines 43-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of AAPA by including a pnn-photodiode region as taught by Maegawa, in order to prevent the deterioration of the sensitivity due to expansion of the depletion layer in the depth direction (col. 3, lines 36-61).

Regarding claims 4 and 7, although the combination of AAPA and Maegawa fails to disclose the doping concentration of the n/p photodiode region, this does not define patentable over AAPA and Maegawa since the doping concentration of the n/p photodiode region is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific doping concentration of the n/p photodiode region does not

Art Unit: 2818

provide any critical or unexpected results to an integrated circuit structure. Rather, it is merely an obvious design choice determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Vu

January 31, 2005